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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,495	02/07/2001	Marquette John Anderson	TI-30831	8073

23494 7590 03/12/2007

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
LESNIEWSKI, VICTOR D	
ART UNIT	**PAPER NUMBER**
2152	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
2 MONTHS	03/12/2007	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/778,495
Filing Date: February 07, 2001
Appellant(s): ANDERSON ET AL.

Alan Lintel, Reg. No. 32478
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/18/2006 appealing from the Office action mailed 4/17/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,161,162	DEROO ET AL.	12-2000
6,016,525	CORRIGAN ET AL.	1-2000
5,887,146	BAXTER ET AL.	3-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-6, 8, 10, 11, 13, 14, and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeRoo et al. (U.S. Patent Number 6,161,162), hereinafter referred to as DeRoo, in view of Corrigan et al. (U.S. Patent Number 6,016,525), hereinafter referred to as Corrigan.

DeRoo disclosed a multiprocessing computer system providing multiplexed address and data paths from multiple CPUs to a single storage device. In an analogous art, Corrigan

disclosed a system wherein a master device is able to perform loopback testing of an integrated circuit.

Concerning claims 1, 8, and 13, DeRoo did not explicitly state selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to said system memory in a normal mode and wherein accesses directed towards the system memory are passed to said shared memory in a verification mode. However, Corrigan does explicitly disclose this feature as his system provides loopback testing wherein a signal directed toward overlapping address space is passed to a shared memory. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of DeRoo by adding the ability to selectively pass system memory accesses either to the system memory or the shared memory responsive to the signal as provided by Corrigan. Here the combination satisfies the need for more effective testing of integrated circuits and devices. See Corrigan, column 2, lines 15-24.

Some claims will be discussed together. Those claims which are essentially the same except that they set forth the claimed invention as a method are rejected under the same rationale applied to the described claim.

Thereby, the combination of DeRoo and Corrigan discloses:

- <Claims 1 and 8>

  A processing device comprising: a master processor; a system memory; a slave processor subsystem including: a slave processor; a shared memory accessible by said master processor and said slave processor (DeRoo, column 2, lines 13-31); and an external memory interface allowing said slave processor to access said system memory (DeRoo,

column 8, lines 21-30); circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device (DeRoo, column 20, lines 15-25) or verification mode for testing the processing device (DeRoo, column 19, lines 29-38); and a verification interface for selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to said system memory in a normal mode and wherein accesses directed towards the system memory are passed to said shared memory in a verification mode (Corrigan, column 2, line 50 through column 3, line 31).

- <Claims 4, 10, and 11>

  The processing device of claim 1 wherein said verification interface comprises multiplexing circuitry for passing data to said external memory interface from either said system memory or said shared memory responsive to whether said verification interface is in a normal mode or a verification mode (DeRoo, column 82, lines 7-39).

- <Claim 5>

  The processing device of claim 4 and further comprising a control interface coupled between said master processor and said shared memory (DeRoo, column 2, lines 18-24).

- <Claim 6>

  The processing device of claim 5 wherein said multiplexing circuitry comprises first multiplexing circuitry and further comprising second multiplexing circuitry for passing control signals to said control interface from either said master processor or said external memory interface responsive to whether said verification interface is in a normal mode or a verification mode (DeRoo, column 83, lines 28-44).

- <Claim 13>

  A processing device comprising: a master processor; a system memory; a slave processor subsystem including: one or more slave processors; a shared memory accessible by said master processor and said slave processors (DeRoo, column 2, lines 13-31); circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device (DeRoo, column 20, lines 15-25) or verification mode for testing the processing device (DeRoo, column 19, lines 29-38); and a system memory interface allowing said slave processors to access said system memory (DeRoo, column 8, lines 21-30); and a verification interface for selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to said system memory in a normal mode and wherein accesses directed towards the system memory are passed to said shared memory in a verification mode (Corrigan, column 2, line 50 through column 3, line 31).

- <Claim 14>

  The processing device of claim 13 wherein said system memory interface comprises: respective external memory interfaces associated with each slave processor; and a memory arbiter for arbiting between memory accesses generated by each of said external memory interfaces (DeRoo, column 2, lines 13-31).

- <Claim 17>

  The processing device of claim 13 wherein said verification interface comprises multiplexing circuitry for passing data to said system memory interface from either said

system memory or said shared memory responsive to whether said verification interface is in a normal mode or a verification mode (DeRoo, column 82, lines 7-39).

- <Claim 18>

  The processing device of claim 17 and further comprising a control interface coupled between said master processor and said shared memory (DeRoo, column 2, lines 18-24).

- <Claim 19>

  The processing device of claim 18 wherein said multiplexing circuitry comprises first multiplexing circuitry and further comprising second multiplexing circuitry for passing control signals to said control interface from either said master processor or said system memory interface responsive to whether said verification interface is in a normal mode or a verification mode (DeRoo, column 83, lines 28-44).

Since the combination of DeRoo and Corrigan discloses all of the above limitations, claims 1, 4-6, 8, 10, 11, 13, 14, and 17-19 are rejected.

Claims 2, 3, 7, 9, 12, 15, 16, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeRoo in view of Corrigan, as applied above, further in view of Baxter et al. (U.S. Patent Number 5,887,146), hereinafter referred to as Baxter.

The combination of DeRoo and Corrigan disclosed a multiprocessing computer system providing multiplexed address and data paths from multiple CPUs to a single storage device that includes loopback testing capabilities. In an analogous art, Baxter disclosed a system for improving the efficiency of operation in multiprocessor systems using a cache coherency protocol. See column 7, lines 15-25.

Although the combination of DeRoo and Corrigan did not explicitly state the inclusion of a cache coupled to the external memory controller and a slave processor or a protocol translator, Baxter taught both a cache memory and the translation of protocols. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of DeRoo and Corrigan by adding a cache and the ability to translate protocols as provided by Baxter. This would make sense because it would improve the efficiency of operation of the system which is a well known need in the art.

Thereby, the combination of DeRoo, Corrigan, and Baxter discloses:

- <Claim 2>

  The processing device of claim 1 wherein said slave processor subsystem further includes a cache memory coupled to said external memory controller and said slave processor (Baxter, column 4, line 67 through column 5, line 21).

- <Claims 3 and 9>

  The processing device of claim 1 wherein said verification interface includes a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory (Baxter, column 5, lines 34-37).

- <Claims 7 and 12>

  The processing device of claim 6 and further comprising a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory (Baxter, column 5, lines 34-37).

- <Claim 15>

  The processing device of claim 13 wherein said slave processor subsystem further includes cache memories associated with each of said slave processors (Baxter, column 4, line 67 through column 5, line 21).

- <Claim 16>

  The processing device of claim 13 wherein said verification interface includes a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory (Baxter, column 5, lines 34-37).

- <Claim 20>

  The processing device of claim 19 and further comprising a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory (Baxter, column 5, lines 34-37).

Since the combination of DeRoo, Corrigan, and Baxter discloses all of the above limitations, claims 2, 3, 7, 9, 12, 15, 16, and 20 are rejected.

(10) Response to Argument

In the brief, the appellant has argued:

- <Argument 1>

  The combination of DeRoo and Corrigan does not disclose the features of independent claim 1 and like independent claims because it does not disclose "a master processor" and "a slave processor subsystem" as recited in claim 1.

- <Argument 2>

  The combination of DeRoo and Corrigan does not disclose the features of independent claim 1 and like independent claims because it does not disclose "circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device or verification mode for testing the processing device" as recited in claim 1.

- <Argument 3>

  The combination of DeRoo and Corrigan does not disclose the features of independent claim 1 and like independent claims because it does not disclose "a verification interface for selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to said system memory in a normal mode and wherein accesses directed towards the system memory are passed to said shared memory in a verification mode" as recited in claim 1.

In response to argument 1 (set forth on page 15 of the brief, second and third paragraphs under the heading "Claims 1, 8, and 13"), the combination of DeRoo and Corrigan does disclose the master processor and slave processor subsystem as recited in claim 1. First turning to the master processor, the previous line citation to DeRoo, column 2, lines 13-31, clearly states the

use of a primary CPU. Such a CPU meets the limitation of the claims as "a master processor" is not further described in the claims so as to distinguish it from such a CPU in DeRoo's system. See, for example, DeRoo's item 702 of figure 20. Concerning the slave processor subsystem, the previous line citation to DeRoo, column 2, lines 13-31, clearly states the use of a controller, a common memory, and interfaces between the controller and the memory device. DeRoo's system control processor (SCP) meets the limitation of the claims as "a slave processor". See DeRoo's item 706 of figure 20. DeRoo's common memory meets the limitation of the claims as "a shared memory accessible by said master processor and said slave processor". See DeRoo's item 704 of figure 20. DeRoo's human user-input interface (HUI) meets the limitation of the claims as "an external memory interface allowing said slave processor to access said system memory". See DeRoo's item 700 of figure 20. See also DeRoo, column 4, lines 11-15 and column 36, line 1 through column 37, line 5, which describe the HUI and DeRoo, column 57, lines 38-42, which also shows that the HUI allows the SCP to communicate with the CPU (containing system memory) in addition to effectuating access of the common memory by both the master processor (CPU) and the slave processor (SCP). The circuitry and verification interface elements of the slave processor subsystem will be discussed in more detail below in response to arguments 2 and 3.

Further, items 706, 704, and 700 of DeRoo's figure 20 clearly make up "a slave processor subsystem" as presented in the claims. The appellant has argued that "the shared memory (704) is not part of a slave processor subsystem" but has given no support as to how this conclusion was drawn. Clearly the SCP (item 706), the SCP interface present in the HUI (item 700), and the common memory (item 704) all function together to effectuate access and control of the common

memory and to allow certain communications to and from the CPU. Thus, it is maintained that these items make up a slave processor subsystem. The term has not been further described in the claims so as to distinguish it from these items.

In response to argument 2 (set forth in the last paragraph of page 15 of the brief), the combination of DeRoo and Corrigan does disclose the circuitry as recited in claim 1. The previous line citations to DeRoo, column 20, lines 15-25 and column 19, lines 29-38, clearly state the use of different signals used for different modes of operation. The first citation (column 20) discusses signals in normal modes of operation while the second citation (column 19) states the use of an ISOLATE signal which can effectuate a test mode. The appellant has argued that the ISOLATE signal can be used at other times, however, it is contended that just because DeRoo teaches alternate uses for a given signal in a more detailed system than the appellant's, this does not mean that he does not also teach signals to effectuate a test mode. DeRoo specifically states putting his system into a test mode, thereby it is clear that his system maintains circuitry for differentiating between a normal mode and a test mode.

In response to argument 3 (set forth on pages 16-18 of the brief), the combination of DeRoo and Corrigan does disclose the verification interface as recited in claim 1. The previous line citation to Corrigan, column 2, line 50 through column 3, line 31, clearly states the enablement of a loopback operation during which a data transfer to a second bus is redirected to shared memory. The loopback mode is a verification mode as it improves the testability of the

circuit by using the shared memory interface to test downstream transactions. See also the discussion of figure 2 at column 5, line 64 through column 6, line 27.

Corrigan's downstream transactions are addressed as though normally destined for the secondary PCI bus, but in loopback (or verification) mode the configuration parameters allow the transaction to be directed to the shared memory. It is maintained that one of ordinary skill in the art would have easily been able to apply the knowledge of Corrigan's loopback operation to a similar system such as that of DeRoo. DeRoo's SCP communicates with the CPU (on a second bus). With knowledge of Corrigan's loopback operation one could easily see how such a communication could be directed to the common memory instead of arriving at the CPU. Looking at the loopback operation of figure 2 in Corrigan, one of ordinary skill could take this concept and easily extend it to any system with communications between two processors and a shared memory.

Concerning the appellant's specific remarks, the appellant argues in detail that "Corrigan shows two paths available for a device on the primary bus 252 to access a single shared memory 202 which exists external to the bridge circuit." Thus the appellant seems to contend that Corrigan does not teach accessing a system memory in a normal mode as his accesses are only intended for a device on a second bus. Here it is noted that the rejection is based on the combination of DeRoo and Corrigan and that the combination would clearly teach a CPU with a system memory on the second bus as DeRoo clearly teaches communications between the SCP and CPU as discussed above. The appellant is reminded that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of

references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Thus, it is clear that the combination of DeRoo and Corrigan teaches the verification interface as Corrigan supplements the teachings of DeRoo by clearly teaching communications from a device on a first bus to a device on a second bus in a normal mode and communications from a device on a first bus to a device on a second bus that are directed to a shared memory in a loopback (or verification) mode. Thus, the appellant's argument that "combining DeRoo with Corrigan would only result in a device having a master processor that could access a single memory using one of two possible paths" is nonsensical. As the appellant admits on page 16 "the PCI bridge 2 in Corrigan allows devices on the secondary PCI bus 256 to communicate with devices on the primary PCI bus 252, and vice versa" and on page 17, discussing the access request which is eventually directed to the shared memory in loopback mode, "the PCI bridge 2 will see this as a request to access a device on the secondary bus 256 through the PCI bridge 2." Taking into account the loopback operation (which was well known in the art at the time of the applicant's invention as disclosed by Corrigan) in combination with DeRoo's system of multiple processors and a common memory, the combination of DeRoo and Corrigan discloses all the limitations of claim 1 and like independent claims.

For the above reasons, it is believed that the rejections should be sustained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Respectfully submitted,

Victor Lesniewski
Patent Examiner
Group Art Unit 2152

Dated: March 8, 2007

BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER

Conferees:

Lynne H. Browne
Appeal Specialist, TQAS
Technology Center 2100